Attorney Docket No. 13054-285A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:	)	
	)	Before the Examiner
James A. Cooper et al.	)	
	)	Phuc T. Dang
Serial No. 12/429,176	)	
	)	Group Art Unit 2892
Filed April 23, 2009	)	
	)	
SiC POWER DMOSFET WITH	)	
SELF-ALIGNED SOURCE CONTACTS	)	
AND METHOD FOR MAKING THE SAME	)	

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/R. Randall Frisk /
R. Randall Frisk, Reg. No. 32,221

AMENDMENT AFTER FIRST ACTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please enter the following amendment in response to the February 23, 2011 Office Action. Please provide any extension of time which may be necessary and charge any fees which may be due for extra claims or otherwise, except for the issue fee, to Deposit Account No. 50-2176.

REMARKS

Reconsideration of the application, as amended, is respectfully requested.

The present application contains claims 2, 4, 6 and 8-18, of which, claims 4-18 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite, and claim 2, 4 and 6 stand rejected under 35 U.S.C. §103(a) in view of Miura (claims 4 and 6) and over Kumar in view of Miura (claim 2). Applicant's response will be made with reference to the examiner's paragraph numbers.

Drawings

5. The examiner objected to the drawings, stating that Figs. 1 and 2 fail to include the label "Prior Art" and that no figure shows "a polysilicon gate above each of the first and second oxide layer as claimed in claim 4."

Regarding the request to label Figures 1 and 2 as "Prior Art", applicant respectfully suggests that such wording would be improper. While the semiconductor device depicted in Figure 1 (and later in Figure 2) is identified as a "conventional DMOSFET 11[1], applicant intends only to show therein problems associated with some MOSFETs (such as misalignment of source contact masks and minimizing specific-on resistance). Applicant has not contended that all elements and features of the devices depicted in Figures 1 and 2 are in the prior art, and labeling Figures 1 and 2 as "prior art" would therefore be improper. Applicant respectfully requests that the objection to Figures 1 and 2 for failure to label as "Prior Art" be withdrawn.

Regarding the examiner's statement that there is no figure showing "a polysilicon gate above each of the first and second oxide layers", there are several figures which show the claimed limitation. For example, reference is made to Fig. 3 wherein the "50nm thick silicon lower gate oxide layer 59 [was grown] on top of the entire surface 28 of the SiC substrate body 22"[2], atop which is created at least two gates 38 by "deposition of a 4000 A … layer of polysilicon 66 atop oxide layer 59" followed by etching through a gate mask 62, "thus creating gates38."[3] It is noted that the oxidation layer 59 refers to the layer 59 that is first deposited atop surface 28, but also to any particular part or parts thereof, as modified by corresponding description. Thus, in Fig. 7 the oxide layer 59 is shown as one continuous layer extending atop

[1] Application, page 6, lines 21-22.
[2] Application, page 10, lines 9-11.
[3] Application, page 10, lines 12-16

the entire surface 28 of substrate 23, but any identified portion thereof is also understood to be an oxide layer. Thus, in Fig. 7 there is a gate 38 formed atop a layer of oxide 59. And in Fig. 8, after the oxide layers atop surface 28 and generally between gates 38 have been removed down to surface 28, the remaining oxide layers 59 now exist more specifically below each gate 38. Thus in both Figs. 7 and 8, as well as in Figs. 3 and 4, for each gate 38, there is an oxide layer 59 disposed subjacent thereto.

The drawings are believed to show every feature of the invention, as claimed, and the objection to amend the drawings is respectfully requested to be withdrawn.

Specification.

6. The examiner has objected to the title. The title has been amended, as suggested.

The specification at pages 6 and 10 has also been amended to correct two grammatical errors and to make clearer two aspects of the oxide layer deposition and removal discussed thereat. No new matter is believed to be entered thereby.

Claim Rejections – 35 USC § 112.

7. Claims 4-18 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. More specifically, the examiner states that, in claim 4, line 6, the limitation "a polysilicon gate above each of the first and second oxide layers" is not clearly defined. Applicant respectfully submits that the phrase is clearly defined. That is, there is claimed "a polysilicon gate above each of said first and second oxide layers." Thus, for each oxide layer, there is a polysilicon gate. Since there are "first and second oxide layers on said upper surface…", then there must be at least two polysilicon gates.

Similarly, the examiner states that, in claim 4, line 6, the term " 'a gate oxide layer….' is a single layer, however, in lines 8-9, a term of '…gate oxide layers' are a plural, not a single of 'gate oxide layer' ". As stated above, there is claimed "a polysilicon gate above each of said first and second oxide layers" and "a gate oxide layer … over each of said gates and the sides thereof." Thus, for each oxide layer, there is a polysilicon gate, and for each gate, there is a gate oxide layer. There must therefore be a gate oxide layer for each of the first and second oxide layers, and thus a plurality of gate oxide layers.

Similarly, the examiner states that, in claim 8, line 9, "the term of 'a gate oxide layer….' is a single layer, however, in line 10, a term of '…gate oxide layers' are a plural, not a single of 'gate oxide layer'." As stated above, claim 8 recites "at least two polysilicon gates…each having a top, a bottom and sides…" and "a gate oxide layer … over said tops and sides of each of said gates." Thus, for each polysilicon gate, there is a gate oxide layer. Since there are at least two polysilicon gates, there must therefore be at least two (a plurality) of gate oxide layers.

Independent claims 4 and 8 and the claim 5-7 and 9-18 depending therefrom are believed to be definite and to particularly point out and distinctly claim the subject matter which applicant regards as his invention. Applicant respectfully requests that the rejection of claims 4-18 under 35 USC §112 be withdrawn.

Claim Rejections – 35 USC § 103.

8. Claims 4 and 6 stand rejected under 35 USC § 103 as being unpatentable over Miura. Applicant respectfully submits that the Examiner has not made out a *prima facie* case of obviousness, and that the examiner has failed to provide sufficient reason to modify Miura as suggested by the Examiner.

"The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious."[4] "Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007) (quoting with approval from *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).[5]

"The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art."[6] Post-*KSR*, the Court of Appeals for the Federal Circuit says that we must still be careful not to allow hindsight reconstruction of references to reach the claimed invention. "Some kind of motivation must be shown from some source, so that the jury can understand why

[4] MPEP §2142.
[5] Cited in MPEP §2142.
[6] MPEP §2142 (emphasis added).

a person of ordinary skill in the art would have thought of either combining two or more references or modifying one to achieve the patented method."[7]

The examiner states that Miura discloses the features of the invention of claims 4 and 6, except that it "does not disclose a plurality of gates that are made of polysilicon and the source electrode is made of metal." The examiner's statement of obviousness is that it would have been obvious "to form a plurality of gates are made of polysilicon and the source electrode is made of metal to improve the silicon carbide MOSFET structure, since it has been held within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice," citing *In re Leshin*, 125 USPQ 416.[8]

Applicant traverses the examiner's rejection and respectfully submits that the examiner's rejection fails to provide sufficient reason with a rational underpinning to explain why a person of ordinary skill would make the recited composition choices and that the cited reference does not disclose all the features recited by the examiner.

There is no disclosure, teaching or suggestion in Miura as to what the composition of the gates should be, and the examiner has provided no reason with a rational underpinning to explain why a person of ordinary skill in the art would form the gates of polysilicon. Stating that the selection is a matter of design choice and "within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use" is conclusory, is based on impermissible hindsight and ignores the applicant's recognition of problems with prior art semiconductor devices (such as misalignment of source contact masks and minimizing specific-on resistance) and of the benefits realized by the claimed invention.

It should be noted here that, in addition to Miura not disclosing a polysilicon gate or metal electrode, Miura also does not disclose the "a gate oxide layer … over each of said gates", as recited in claim 4. Miura instead discloses only an "inter-layer insulation film 7, and nowhere teaches or suggests the composition of such film 7. Thus, Miura does not disclose the composition of the gates *or* the insulation film, nor does Miura provide any teaching or suggestion what either the gates or insulation film should be made of or what factors would guide such decisions.

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[7] *Innogenetics v. Abbott Labs,* 512 F.3d 1363, 85 USPQ2d 1641 (Fed. Cir. 2008).
[8] February 23, 2011 Office Action, page 5.

It is further noted that, in Fig. 1 of Miura the inter-layer insulation film 7 is *depicted* as being thicker than the gate oxide films 5a, 5b, but Miura nowhere teaches that either of films 5a/5b are to be thicker or thinner than film 7 or that the drawings are intended to be to scale.

In connection with the other limitations of claim 4, applicant's invention provides for a SiC substrate and polysilicon gates because growth of the oxidation layer on the polysilicon gates occurs considerably faster than on the SiC substrate, which creates a much thinner combined oxide layer between adjacent gates (as shown in Fig. 7 of the application) than is simultaneously formed on the tops and sides of such gates. Thus, after a short oxide etch is applied, long enough to completely remove the thin, combined oxide layer over the substrate surface (and between the gates), there is still left a very thick insulating oxide layer on the tops and sides of gates. This is more than an obvious design choice and is nowhere disclosed, taught or suggested by Miura.

It is respectfully submitted that the examiner's rejection fails to articulate sufficient reasoning with some rational underpinning to explain why a person of ordinary skill would create gates made of polysilicon and first and second oxide layers therebelow in connection with the MOSFET with a SiC substrate and metal electrode, as recited in claim 4.

For the foregoing reasons, Applicant respectfully submits that the inventions of independent claim 4 and of claim 6 depending therefrom are patentable over Miura.

9. Claim 2 stands rejected under 35 USC § 103 as being unpatentable over Kumar et al. in view of Miura. Applicant respectfully submits that the Examiner has not made out a *prima facie* case of obviousness, and that there is no apparent reason to modify Kumar as suggested by the Examiner.

The examiner's statement of obviousness is that it would have been obvious "to modify the teaching of Kumar to provide the second oxide layer is thicker than the first oxide layer as taught by Miura for the purpose of improving a silicon carbide power MOSFET."[9]

It is respectfully submitted that the purpose of "improving a silicon carbide power MOSFET" does not constitute sufficient reason to change the basic structure of the Kumar semiconductor device.[10] Improving upon the prior art devices is the purpose of all inventions sought to be patented and would not provide a jury any useful guidance to understand why a

[9] February 23, 2011 Office Action, page 6.
[10] *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007)

person of ordinary skill in the art would have thought of modifying Kumar to achieve the invention of claim 2.

Moreover, applicant suggests that Miura does not teach the purported size relationship, and it would therefore be improper to so modify the Kumar semiconductor device. In Fig. 1 of Miura the inter-layer insulation film 7[11] is *depicted* as being thicker than the gate oxide films 5a, 5b, but Miura nowhere teaches that either of the gate oxide films 5a/5b are to be thicker or thinner than the inter-layer insulation film 7 or that the drawings are intended to be to scale. Thus is it submitted that Miura teaches nothing about the relative sizes of a gate oxide film below a gate and an insulation film above and/or on the sides of a gate in semiconductor device.

It is respectfully submitted that there is no reason to combine the teachings of Miura to the Kumar semiconductor device and that, even if the teachings of Miura were applied to the Kumar device, there are no teachings in Miura that would suggest to a person of ordinary skill in the art to make the second oxide layer of the Kumar device thicker than its first oxide layer.

For the foregoing reasons, Applicant respectfully submits that the invention of claim 2 is patentable over Kumar in view of Miura.

Amended Claims

Applicant acknowledges claims 5 and 7 have been indicated to be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 5 and 7 have been so rewritten, and their allowance is respectfully requested.

In view of the foregoing remarks and amending changes, claims 2 and 4-18 are believed to be in condition for allowance, and such action is respectfully requested. The Examiner is invited to call the undersigned attorney if there are any remaining issues to be discussed.

Respectfully submitted,

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[11] The inter-layer insulation film 7 is not disclosed as being an oxide layer.